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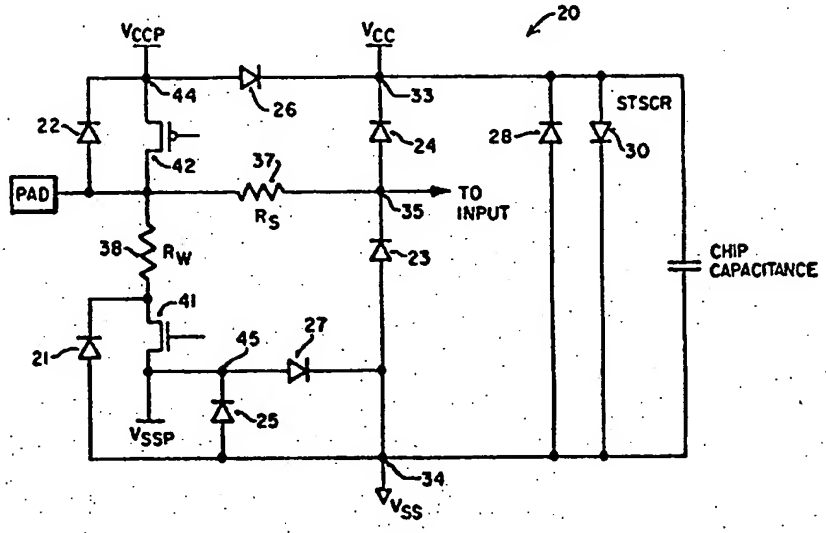
(54) Title: ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT



(57) Abstract

A device for protecting an integrated circuit (IC) against electrostatic discharge (ESD) includes a self-triggered silicon controlled rectifier (STSCR) coupled across the internal supply potentials (Vcc, Vss) of the integrated circuit. The STSCR exhibits a snap-back in its current versus voltage characteristic which is triggered at a predetermined voltage during an ESD event. As large voltages build up across the chip capacitance, the predetermined voltage of the SCR (30) is triggered at a potential which is sufficiently low to protect the internal junctions of the IC from destructive reverse breakdown. The STSCR comprises a pnpn semiconductor structure which includes an n-well disposed in a p-substrate. A first n+ region (62) and p-type region (64) are both disposed in the n-well (60). The n+ and p-type regions are spaced apart and electrically connected to form the anode of the SCR. The ESD protection device also includes diode clamps (26, 27) between the periphery and internal power supply lines, and a novel well resistor which provides a distributed resistance further protecting sensitive output buffer circuitry.